IN THE CLAIMS

Please amend the specification as follows.

1. (Currently Amended) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary ~~code~~ outputs indicating the number of binary ones in the plurality of binary inputs, said plurality of outputs including a first output adapted to output a least significant bit of the binary outputs and at least one other output adapted to output at least one higher significant bit of the binary outputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating each at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the elementary EXOR symmetric function comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if $m \geq \geq 1$ and the number of inputs is an odd number or AND logic combining sets of one or more binary inputs and EXOR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if $m \geq \geq k$ and the number of sets of inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, said sets of binary inputs are a cover of all possible combinations of binary inputs and are each unique sets, said logic circuit is divided into a plurality of EXOR logic units, each EXOR logic unit is arranged to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

2. (Previously Presented) A parallel counter according to claim 1 wherein said logic circuit is arranged to generate at least one of the binary outputs as an elementary OR symmetric function of the binary inputs, and is divided into a plurality of OR logic units, the binary inputs

of said plurality of inputs are divided according to a binary tree into inputs into a plurality of said OR logic units, each OR logic unit is arranged to generate at least one logic unit binary output as an elementary OR symmetric function of the binary inputs to the OR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said OR logic units, at least one binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said OR logic units, and the elementary OR symmetric function comprises the result of OR logic combining binary inputs to generate a binary output which is high if and only if m ≥ ≥1 or AND logic combining sets of binary inputs and OR logic combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m ≥ ≥k, and each set being unique and the sets covering all possible combinations of binary inputs.

3. (Currently Amended) A parallel counter according to claim 2, wherein said OR logic units are arranged to receive 2^n of said binary inputs, where n is an integer indicating the level of the OR logic units in the binary tree, said elementary OR symmetric function logic ~~circuit~~ has ~~m~~ p OR logic units at each level, where ~~m~~ p is a rounded up integer determined from (the number of binary inputs)/ 2^n, OR logic units having a higher level in the binary tree comprise logic of OR logic units at lower levels in the binary tree, and each OR logic unit is arranged to generate logic unit binary outputs as an elementary OR symmetric function of the binary inputs to the OR logic unit.

4. - 15. (Canceled)

16. (Currently Amended) A logic circuit for multiplying two binary numbers comprising:

array generation logic for generating an array of binary numbers comprising ~~all possible~~ combinations of bits ~~each bit~~ of each binary number;

array reduction logic including at least one parallel counter for reducing the number of combinations in the array; and

binary addition logic for adding the reduced combinations to generate an output;

wherein at least one said parallel counter comprises:

~~a plurality of~~ at least five inputs for receiving ~~a binary number as~~ a plurality of binary inputs;

~~a plurality of~~ at least three outputs for outputting binary ~~code~~ outputs indicating the number of binary ones in the plurality of binary inputs, said at least three outputs including a first output for outputting a least significant bit of the binary outputs and at least one other output for outputting at least one higher significant bit of the binary outputs; and

a logic circuit connected between the ~~plurality of~~ inputs and the ~~plurality of~~ outputs and for generating at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the logic circuit comprises elementary EXOR symmetric function logic comprising ~~comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or~~ AND logic for combining sets of ~~one or more~~ binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set is unique, the sets cover all possible combinations of binary inputs, said elementary EXOR symmetric function logic [circuit] is divided into a plurality of EXOR logic units, each EXOR logic unit ~~is arranged~~ includes logic to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said ~~plurality of~~ at least five inputs are divided into inputs into a plurality of said EXOR logic units, and at least one said higher significant bit of the binary ~~output of said plurality of~~ outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

17. (Currently Amended) A method of designing a logic circuit comprising:

providing a library of logic module designs each for performing a ~~small~~ symmetric function;

designing a logic circuit to perform a large symmetric function comprising a symmetric function having a larger number of inputs that said symmetric functions performed by said logic module designs;

identifying ~~small~~ symmetric functions ~~which can perform~~ for the performance of said large symmetric function;

selecting logic ~~modules~~ module designs from said library to perform some of said ~~small~~ identified symmetric functions;

identifying ~~a~~ at least one logic ~~circuit~~ module design in the selected logic ~~circuit~~ module designs which performs a symmetric function ~~and~~ which has a relationship to ~~can be used to perform~~ another symmetric function for the performance of said large symmetric function; and

~~selecting the logic circuit corresponding to the identified symmetric function and~~ using said at least one identified ~~the selected~~ logic module design ~~circuit~~ with inverters to perform said other symmetric function using the relationship between the symmetric functions:

$$OR\_n\_k(X_1...X_n) = \neg OR\_n\_(n+1-k)(\neg X_1...\neg X_n)$$

where $\neg$ denotes an inversion, n is the number of inputs, and k is the number of sets of inputs AND combined together.

18. (Currently Amended) A conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter comprising a parallel counter for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater than 2^p, and said parallel counter comprises:

~~a plurality of~~ at least five inputs for receiving ~~a binary number as~~ a plurality of binary inputs;

~~a plurality of~~ at least three outputs for outputting binary ~~code~~ outputs indicating the number of binary ones in the plurality of binary inputs, said plurality of outputs including a first output for outputting a least significant bit of the binary outputs and at least one other output for outputting at least one higher significant bit of the binary outputs; and

a logic circuit connected between the ~~plurality of~~ inputs and the ~~plurality of~~ outputs and for generating at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the logic circuit comprises elementary EXOR symmetric function logic comprising ~~comprises the result of EXOR logic combining the binary inputs to generate a binary~~

~~output which is high if and only if m >1 and the number of inputs is an odd number or~~ AND logic for combining sets of ~~one or more~~ binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m ≥ ≥k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set is unique, the sets cover all possible combinations of binary inputs, said elementary EXOR symmetric function logic ~~circuit~~ is divided into a plurality of EXOR logic units, each EXOR logic unit ~~is arranged~~ includes logic adapted to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one said higher significant bit of the binary ~~output of said plurality of~~ outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

19. (Currently Amended) A constant multiplier comprising a conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter comprising a parallel counter for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater than 2^p,and said parallel counter comprises:

~~a plurality of~~ at least five inputs for receiving ~~a binary number as~~ a plurality of binary inputs;

~~a plurality of~~ at least three outputs for outputting binary ~~code~~ outputs indicating the number of binary ones in the plurality of binary inputs , said outputs including a first output for outputting a least significant bit of the binary outputs and at least one other output for outputting at least one higher significant bit of the binary outputs; and

a logic circuit connected between the ~~plurality of~~ inputs and the ~~plurality of~~ outputs and for generating at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the logic circuit comprises elementary EXOR symmetric function logic comprising ~~comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or~~ AND logic for combining sets of ~~one or more~~ binary inputs and EXOR logic combining the AND logic

combined sets of binary inputs to generate a binary output which is high if and only if m ~~≥~~ ≥k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set is unique, the sets cover all possible combinatios of binary inputs, said elementary EXOR symmetric function logic ~~circuit~~ is divided into a plurality of EXOR logic units, each EXOR logic unit ~~is arranged~~ includes logic adapted to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one said higher significant bit of the binary output of said plurality of outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

20. (Currently Amended) A digital filter comprising a conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter comprising a parallel counter for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater than 2^p, and said parallel counter comprises:

~~a plurality of~~ at least five inputs for receiving a binary number as a plurality of binary inputs;

~~a plurality of~~ at least three outputs for outputting binary ~~code~~ outputs indicating the number of binary ones in the plurality of binary inputs , said outputs including a first output for outputting a least significant bit of the binary outputs and at least one other output for outputting at least one higher significant bit of the binary outputs; and

a logic circuit connected between the ~~plurality of~~ inputs and the ~~plurality of~~ outputs and for generating at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs;

wherein the logic circuit comprises elementary EXOR symmetric function logic comprising ~~comprises the result of EXOR logic combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of inputs is an odd number or~~ AND logic for combining sets of ~~one or more~~ binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m ~~≥~~ ≥k and the number of sets of high inputs is an odd number, where m is the number of high

inputs and k is the size of the sets of binary inputs, , each set is unique, the sets cover all possible combinations of binary inputs, said elementary EXOR symmetric function logic ~~circuit~~ is divided into a plurality of EXOR logic units, each EXOR logic unit ~~is arranged~~ includes logic to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one said higher significant bit of the binary ~~output of said plurality of~~ outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

21. (Currently Amended) A parallel counter comprising:

at least five inputs for receiving ~~a binary number as~~ a plurality of binary inputs;

at least three outputs for outputting binary ~~code~~ outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the ~~plurality of~~ inputs and the ~~plurality of~~ outputs and for generating at least two of the plurality of binary outputs as elementary EXOR symmetric function functions of the binary inputs,

wherein the logic circuit comprises elementary EXOR symmetric function logic comprising at least one of first ~~comprises the result of~~ EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m ≥ ≥1 and the number of high inputs is an odd number, and ~~or~~ AND logic for combining sets of ~~one or more~~ binary inputs and second EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m ≥ ≥k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs .

22. (Currently Amended) A parallel counter according to claim 21 wherein said elementary EXOR symmetric function logic ~~circuit~~ is arranged to generate first and second binary outputs as elementary EXOR symmetric functions of the binary inputs.

23. (Currently Amended) A parallel counter according to claim 22 wherein said first EXOR logic ~~circuit~~ is adapted ~~arranged~~ to generate the first binary output ~~as the elementary EXOR symmetric function comprising the result of EXOR logic combining the binary inputs~~, and said AND logic and said second EXOR logic are adapted to generate the second binary output ~~as the elementary EXOR symmetric function comprising the result of AND logic combining members of each set of binary inputs and exclusively OR logic combining the result of the AND operations~~.

24. (Currently Amended) A parallel counter according to claim 21 wherein said first EXOR logic ~~circuit~~ is arranged to generate the first binary output ~~by EXOR logic combining the binary inputs to and~~ , said AND logic is adapted to generate at least one $(i+1)^{th}$ binary output by AND logic combining 2^i of the binary inputs in each set, and said EXOR logic is adapted to combine ~~combining~~ the result of the AND logic combinations, where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance of a binary output~~, each set being unique and the sets covering all possible combinations of binary inputs~~.

25. (Canceled)

26. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit ~~is arranged~~ includes elementary OR symmetric function logic to generate at least one of the binary outputs as an elementary OR symmetric function of the binary inputs, wherein the elementary OR symmetric function logic comprises ~~the result~~ at least one of OR logic for combining binary inputs to generate a binary output which is high if and only if m ~~≥~~ ≥1 ~~or~~ , and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m ~~≥~~ ≥k, each set being unique and the sets covering all possible combinations of binary inputs.

27. (Canceled)

28. (Currently Amended) A parallel counter according to claim 26 wherein said elementary OR symmetric function logic ~~circuit~~ is arranged to generate the N^{th} binary output as an elementary OR symmetric function, wherein said AND logic is arranged to ~~comprising the result of~~ AND logic ~~combining~~ combine 2^{N-1} of the binary inputs in each set and said OR logic is arranged to OR logic ~~combining~~ combine the AND logic combined sets of binary inputs, where N is the number of binary outputs and the N^{th} binary output is the most significant~~, each set being unique and the sets covering all possible combinations of binary inputs~~.

Claim 29 (Canceled)

30. (Currently amended) A parallel counter according to claim 21 wherein said elementary EXOR symmetric function logic ~~circuit~~ is arranged to generate a first binary output as an elementary EXOR symmetric function of the binary inputs, and said logic circuit includes elementary OR symmetric function logic to generate an N^{th} binary output as an elementary OR symmetric function of the binary inputs, wherein the elementary OR symmetric function logic comprises at least one of first ~~the result of~~ OR logic for combining binary inputs to generate a binary output which is high if and only if m ≥ ≥1, and ~~or~~ AND logic for combining sets of binary inputs and second OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m ≥ ≥k, each set being unique and the sets covering all possible combinations of binary inputs.

31. (Currently Amended) A parallel counter according to claim 21 wherein said logic circuit ~~is arranged~~ includes elementary OR symmetric function logic to generate ~~two~~ a plurality of possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, where N is the number of binary outputs, the sets used for each possible binary output being of ~~two~~ different sizes which are a function of the binary output being generated; and ~~said logic circuit including~~ selector logic to select one of the possible binary outputs based on a more significant binary output value.

32. (Currently Amended) A parallel counter according to claim 31 wherein said elementary OR symmetric function logic ~~circuit~~ is arranged to generate the ~~two~~ possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively and said selector logic being arranged to select one of the possible binary outputs based on the N^{th} binary output value.

33. (Currently Amended) A parallel counter according to claim 21 wherein said AND logic ~~circuit includes~~ and said EXOR logic include a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary ~~OR or~~ EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

34. - 41. (Canceled)

42. [New] A logic circuit for multiplying two binary numbers, the logic circuit comprising:

array generation logic for logically combining bits of the binary numbers to generate an array of logical combinations;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the binary inputs; and

a logic circuit connected between the inputs and the outputs and for generating at least two of the binary outputs as elementary EXOR symmetric functions of the binary inputs,

wherein said logic circuit comprises elementary EXOR symmetric function logic comprising at least one of first EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and

AND logic for combining sets of binary inputs and second EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.

43. [New] A parallel counter comprising:

at least five input means for receiving binary inputs;

at least three output means for outputting binary outputs indicating the number of binary ones in the binary inputs, said output means including a first output for outputting a least significant bit of the binary outputs and at least one other output for outputting at least one higher significant bit of the binary outputs; and

logic means for receiving the binary inputs and for generating at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs; wherein said elementary EXOR symmetric function is a function of the EXOR logic combination of the binary inputs and is high if and only if m $\geq$1 and the number of high inputs is an odd number, or a function of the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if m $\geq$k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said logic means comprises a plurality of EXOR logic means, each EXOR logic means is arranged to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic means, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic means, and at least one said higher significant bit of the binary outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic means.

44. [New] A parallel counter comprising:

at least five inputs for receiving binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the binary inputs, said outputs including a first output for outputting a least significant bit of the binary outputs and at least one other output for outputting at least one higher significant bit of the binary outputs; and

a logic circuit for receiving the binary inputs and for generating at least one of said at least one higher significant bit of the binary outputs as an elementary EXOR symmetric function of the binary inputs; wherein said elementary EXOR symmetric function is a function of the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$ and the number of high inputs is an odd number, or a function of the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;

wherein said logic circuit comprises a plurality of EXOR logic units, each EXOR logic unit comprises logic to generate logic unit binary outputs as an elementary EXOR symmetric function of the binary inputs to the EXOR logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said EXOR logic units, and at least one said higher significant bit of the binary outputs is generated using said logic unit binary outputs of a plurality of said EXOR logic units.

45. [New] A parallel counter comprising:

at least five input means for receiving binary inputs;

at least three output means for outputting binary outputs indicating the number of binary ones in the binary inputs; and

logic means for receiving the binary inputs and for generating at least two of the binary outputs as elementary EXOR symmetric functions of the binary inputs; wherein the elementary EXOR symmetric function is a function of the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$ and the number of high inputs is an odd number, or a function of the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of sets of high inputs is

an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.

46. [New] A parallel counter comprising:

at least five inputs for receiving binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the binary inputs; and

a logic circuit connected between the inputs and the outputs and for generating at least two of the binary outputs as elementary EXOR symmetric functions of the binary inputs, wherein the elementary EXOR symmetric function is a function of the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$ and the number of high inputs is an odd number, or a function of the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs.